Design and Modeling of Compact On-Chip Transformer/Balun Using Multi-Level Metal Windings for RF Integrated Circuits

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Abstract - **A compact integrated balun transformer is analyzed that meets the size demand of highly integrated RFICs for the wireless industry. The design of a balun transformer with 4:1 impedance ratio using multi-level windings significantly reduces the silicon area compared to that occupied by an equivalent planar design. Its application is demonstrated in a highly efficient, linear amplifier design which achieved first pass design success.**

I. INTRODUCTION

The use of on-chip passive components has been widely demonstrated to enhance RFIC circuit performances. Design and analysis techniques have also been explored to correlate the performance of the passive components to their geometry and process parameters, aiming at achieving optimal performance of such passive components as spiral inductors [1] and transformers [2]. One aspect that limits their use is the amount of silicon area that is consumed. Overall die size is a direct driver in production cost. The continuing advance of process technologies, such as providing thicker and lower resistivity metals, thicker and low-k dielectric layers, and higher resistivity substrates, make high quality passive components more readily available. It has been demonstrated that significant improvement on inductor Q can be obtained in an enhanced SiGe RF BiCMOS process which utilizes an additional 4µm Al/Cu top metal and 3µm oxide dielectric layer placed above the conventional metal layer configuration seen in the standard BiCMOS process [3].

In this paper, we will present the modeling results on a compact on-chip balun transformer and its application in a RF amplifier design. Using multiple low loss metal layers for its windings, the resulting balun exhibits improved performance and reduced footprint.

II. BALUN CONSTRUCTION AND DESIGN

A balun, used for conversion between single-ended signals and differential signals, is frequently seen in RF circuits employing differential circuit configuration for better noise suppression. A 1:1 on-chip balun can be realized with a pair of inter-wound spiral inductors having the same inductance. A balun can also be used as an impedance transformer when designed with different inductance values for its primary and secondary windings. One use of such a balun transformer is between a high impedance LO driver output to low impedance differential mixer input. There are several ways to realize an on-chip balun transformer with 4:1 impedance ratio. One planar design uses two identical 1:1 baluns placed side-by-side and then connects two primary windings in series and two secondary windings in parallel. Another planar design may have a continuos primary spiral and cut the secondary spiral into two halves and connect them in parallel [2]. To save silicon area, a compact 4:1 balun transformer using multiple metal layers is proposed in [4] and illustrated in Fig.1.

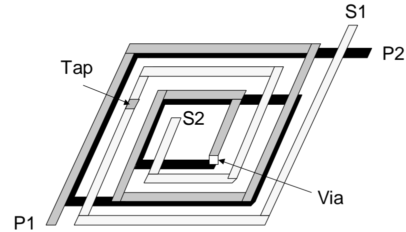

Fig. 1. Compact balun construction.

The primary consists of a winding in two metal layers, while the secondary is on one metal layer only. As a two-level inductor has twice the number of turns and the inductance is proportional to the square of the number of turns, the primary has four times higher inductance than the secondary, hence forming a 4:1 impedance balun transformer. The balun in Fig. 1 can be used for converting singled-ended signal at the primary (high impedance) to a differential signal at the secondary (low impedance), with a center tap located at the electrical center of the secondary winding. With a center tap at the electrical center of the primary winding, it can also be used to convert a differential signal at primary to a single-ended signal at secondary as in the RF amplifier design described in Section III.

The magnetic coupling between the primary and secondary spirals is imperfect (typical magnetic

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coupling coefficient k for on-chip transformers ranges from 0.7 to 0.9), contributing to insertion loss. In addition, the magnetizing inductance due to the finite primary and secondary inductance values causes additional insertion loss, especially at low frequencies. These effects can be effectively compensated for by placing tuning capacitors in shunt with each winding, at the expense of narrowing frequency bandwidth. These tuning capacitors should be selected to resonate out both leakage inductance and magnetizing inductance at the operating frequency, resulting in reduced in-band insertion loss. Note that the parasitic capacitance between the primary top level winding and primary lower level winding, which is in shunt with the primary inductance, can be absorbed by such tuning capacitor. This is in contrast with a stand-alone multi-level inductor whose performance is limited by lower Q and lower self-resonant frequency caused by this inter-level parasitic capacitance. The complete circuit schematic of a balun for converting a single-ended input to a differential output with tuning capacitors is shown in Fig.2, where capacitors C1 and C2 are the tuning capacitors for balun primary and secondary, respectively.

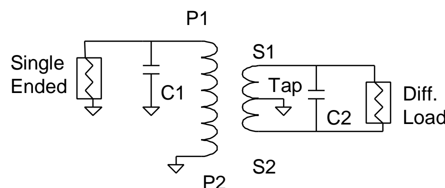

Fig. 2. Balun circuit schematic.

As transformers and baluns are passive components, electromagnetic simulation can be applied to accurately predict their behavior. Improvement in numerical algorithms and computing hardware make electromagnetic simulation increasingly feasible for component modeling and design. Em solvers also provide faster means of exploring novel structures and devices before analytical models can be developed. For compact balun modeling, we used ***em***™, a method-of-moment based planar em solver from Sonnet Software.

The balun design starts with choosing the inductance values for primary and secondary windings, based on required insertion loss, impedance transformation levels, operating frequency, and desired bandwidth. This will be further discussed in Section III. The geometric parameters of the spiral windings are then estimated based on the winding inductance from many readily available analysis tools and empirical formulas. The electromagnetic simulation is then applied. The resulting S-parameter data is used to obtain the tuning capacitors to achieve minimum insertion loss. Finally the S-parameter data and the tuning capacitors are imported into circuit simulators, such as Agilent ADS™ and Cadence SpectreRF™ for use in the overall circuit design.

III. BALUN CHARACTERIZATION

A compact multi-level balun was designed and characterized for converting a 200Ω single-ended input to a 50Ω differential output at 2GHz. The balun was implemented in a SiGe RF BiCMOS process [3]. The primary winding was laid out with 4μm top level metal for its upper half of the primary and next two lower level metals stitched together with many vias (to reduce the winding ohmic loss) for its lower half of the winding. The secondary used the 4μm top metal only. It occupies an area of 350μm x 200μm, which is about one third of the area a planar 4:1 balun would use with the same inductance for the windings using two identical 1:1 baluns described earlier. The em simulation time on the compact multi-level balun took 40 minutes for each frequency on a Pentium III PC with 512MB memory. The complete frequency response from 0.5GHz to 4GHz with a step of 0.25GHz was obtained with an overnight run.

Test structures shown in Fig.3 were designed and fabricated to characterize the baluns and transformers, as well as to validate the em simulation results. Two-port S-parameter on-wafer measurement was conducted on all test cells, as well as on-wafer calibration structures not shown in Fig.3. To characterize the balun configuration which has three terminals (one for single-ended input and two for differential outputs), one of the two differential ports is terminated with a 50Ω on-chip resistor.

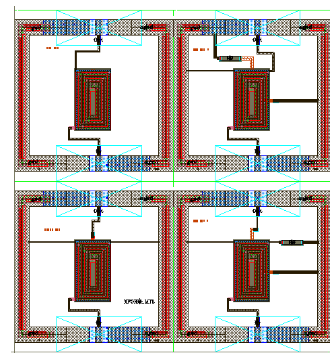

Fig. 3. Balun/transformer test structures.

Figure 4 shows the measured and em simulated S-parameters for the multilayer inductor used as the primary winding for the balun transformer. From these

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data the primary inductance is extracted to be 7.5nH. Figure 5 shows the measured and em simulated result for the transformer configuration where ports P1 and S1 are the input and output ports while P2 and S2 are grounded. Figure 6 shows the two-port measured and simulated results for the balun configuration where P1 and S1 are the measured ports, S2 is connected to an on-chip 50Ω resistor, and P2 and Tap are grounded.

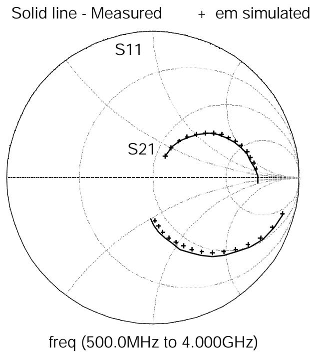

Fig. 4. Measured/simulated results for primary inductor.

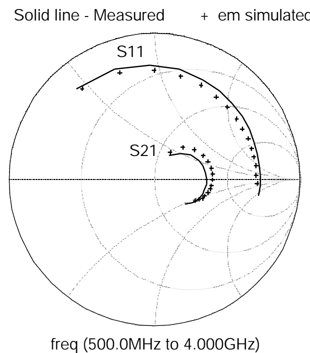

Fig. 5. Measured and simulated results for transformer.

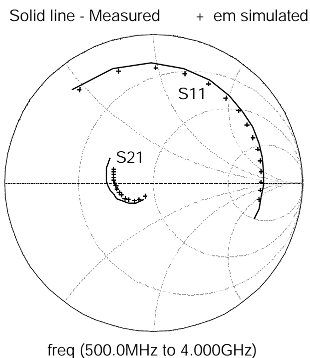

Fig. 6 Measured and simulated results for the balun.

Good agreement from 500MHz to 4GHz between the on-wafer measurement and em simulation data is seen in these figures, which validates the em simulation accuracy. The increasing deviation as the frequency goes higher is partly contributed to the de-embedding procedure, which treats all the feeding lines as stand-alone microstrip lines thus neglecting any coupling among the feeding lines and the spirals.

Figure 7 shows the amplitude and phase responses of the balun differential output based on em simulation data, with port P1 terminated by 200Ω impedance, port S1 and S2 each terminated by 25Ω load (thus 50Ω differentially), and with port P2 and Tap grounded.

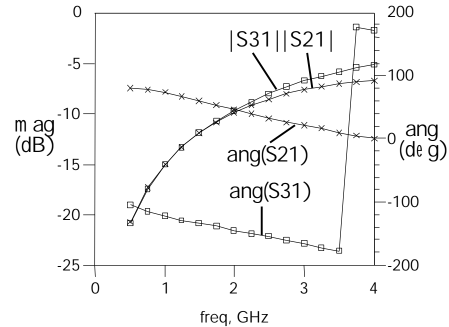

Fig.7. Simulated balun response.

It is seen that the two outputs have very good balance up to 2GHz. The increasing imbalance after that is the result of different high frequency behaviors between inverting (S31) and non-inverting (S21) transmissions explained in [2], mainly due to the parasitic capacitance between the primary and secondary windings. Insertion loss can be further reduced for the operating frequency through the use of tuning capacitors, as shown Fig. 8, where the transmission coefficient S21 from 200Ω single-ended input to 50Ω differential output is shown, using shunt capacitances of 0.5pF and 2.3pF at the input and output, respectively. The insertion loss can be further reduced through the use of larger inner spacing (more square or octagonal winding shape) to give higher Q of the windings; and a narrower line spacing between the primary and secondary to enhance the mutual inductive coupling.

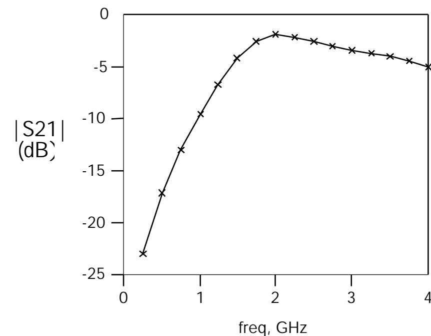

Fig.8. Balun insertion loss after tuning.

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To examine the transformer/balun performance when used with different input and output impedance levels, Fig.9 shows the minimum insertion loss after tuning vs. balun load impedances at 2GHz. Only input impedance is shown on x-axis, while the output impedance is kept ¼ of the input impedance to maintain 4:1 ratio.

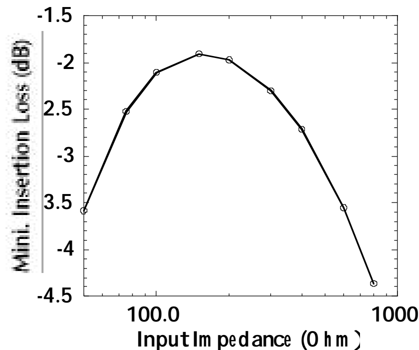

Fig.9. Insertion loss vs. load impedances.

From Fig.9 it is seen that the insertion loss remains relatively flat for the input impedance ranging from 100Ω to 200Ω but increases quickly beyond this range. Recall that the primary inductance is 7.5nH, which corresponds to a reactance of 94Ω at 2GHz. This suggests that the inductance value for the windings can be selected such that the resulting reactance at the operation frequency is about one half (0.5x) to equal to (1x) the impedance levels the winding is connected to. Within this range, the increase in inductance value of the winding improves insertion loss at lower frequencies but occupies larger area. When the load impedance is comparable to the winding internal resistance, any metal ohmic loss of the winding is in series to the load impedance, dissipating power and leading to insertion loss. For higher load impedances, the finite reactance from the windings would make the response further away from ideal transformer. The effect from the parasitic capacitance between the primary and secondary windings is also more pronounced with higher load impedances. Therefore, proper winding inductance should be selected based on the operation frequency and impedance levels to maintain adequate insertion loss.

With a center tap on the electrical center of the primary winding and one side of the secondary grounded, the compact balun can also be used for converting high impedance differential input to single-ended low impedance output. Such a balun was designed and employed in a transmit driver amplifier for use in a portable cellular handset operating in 900MHz frequency range. Connecting 300Ω differential circuitry to 75Ω single-ended first stage amplifier input, the balun occupies an area of 285µm by 285µm and has a 18nH multi-level primary and a 4.5nH single level secondary. With the benefits of using a compact balun including low loss, no current consumption, DC blocking, common mode rejection, this two-stage amplifier design achieved first time design success with high efficiency and high linearity in a small silicon area. Its measured response is shown in Fig.10.

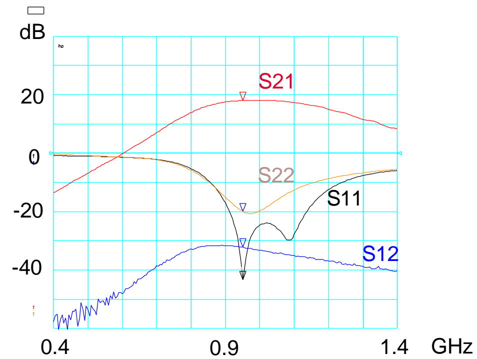

Fig. 10. Amplifier measured response.

IV. CONCLUSION

The availability of multiple low loss metal layers enables more compact passive circuit components. For on-chip transformers/baluns, the resulting higher inductance per unit area from multi-level windings can be used to either reduce the silicon area for the same inductance or use the same silicon area to obtain higher inductance value for improved performance. This paper presented the modeling and characterization results on a compact balun design. Effort of developing compact equivalent circuit model is currently under way so as to enable more efficient circuit design and optimization.

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